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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/818,115	Confirmation No. 1919
Applicant	:	Steven J. Tinsely	
Filed	:	03/27/2001	
TC/A.U	:	2113	
Examiner	:	Joseph D. Manoskey	
Docket No.	:	TI-31546	
Customer No.	:	23494	
Title	:	ACTIVE FAILSAFE DETECTION FOR DIFFERENTIAL RECEIVER CIRCUITS	

APPEAL BRIEF TRANSMITTAL FORM

Mail Stop Appeal Brief – Patents
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Lottie Davis 12-17-04

Lottie Davis Date

Sir:

Transmitted herewith in triplicate is an Appeal Brief in connection with the above-identified application.

Applicants petition for a one month Extension of Time under 37 CFR 1.136. The fee for this extension is $120.00.

12/22/2004 ZJUHAR1 00000038 200668 09818115
01 FC:1402 500.00 DA

12/22/2004 ZJUHAR1 00000038 200668 09818115
02 FC:1251 120.00 DA

Please charge the Appeal Brief fee of $500.00 and the Extension of Time fee of $120.00 and any additional fees in connection with the filing of this paper, including additional extension of time fees to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,
Texas Instruments Incorporated

William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
(972) 917-5452

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Lottie Davis — Date: 12-17-04

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in support of an appeal of the final rejection of Claims 1-20 in connection with the above-identified application. The final Rejection was mailed on 06/21/2004.

REAL PARTY IN INTEREST

The invention has been assigned to Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Applicant's representative which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF THE CLAIMS

Claims 1-20 stand rejected. Claims 1, 3, 8 and 15 were amended in the response to the first Official Action which was mailed on April 8, 2004. No response was filed to the Final Rejection. All claim amendments have been entered.

STATUS OF THE AMENDMENTS

Amendment under 37 C.F.R. 1.111 was mailed on April 8, 2004 and entered. No response was filed to the Final Rejection.

SUMMARY OF THE INVENTION

The present invention relates to a differential bus receiver circuit for data transmission within a computer system, for example. The receiver can be utilized with differential signaling standards such as low voltage differential signaling (LVDS), high voltage differential signaling (HVDS) or other differential signal transmission standards. For a LVDS system, the driver typically includes a current source that drives the differential pair lines in opposition to each other. The differential receiver is provided with a high DC input impedance so that the majority of the driver current flows across a terminating resistor which generates a voltage drop across the receiver input. The changing direction of current flow across the resistor creates a valid digital input signal to the receiver. It is common to have a failsafe feature that provides a predetermined output from the receiver circuit under certain fault conditions on the transmission system. However, these failsafe circuits may generate

false alarm signals in response to signal noise on the transmission line which leads to uncertainty in the state of the receiver output (Page 9, Line 12 through Page 10, Line 16).

The present invention overcomes this technical problem in a simple and elegant manner. A bus activity signal is activated when receiving a differential data signal of sufficient amplitude to transition through a predetermined threshold. A failsafe signal is activated when a low differential voltage condition is detected. A countdown period commences upon activation of either signal, and a failsafe condition is determined to exist if the failsafe signal is active when the countdown time period expires. (Page 11, Line 7 through Page 14, Line 12).

ISSUES

The issues on appeal are whether claims 1-4, 8-11 and 15-18 are unpatentable over Applicant's admitted prior art (hereinafter APA) in view of Erckert, U.S. Patent 6, 493,401; and whether claims 5-7, 12-14, 19 and 20 are unpatentable over the APA and Erckert in view of Shirai, et al., U. S. Patent 5,867, 775.

GROUPING OF THE CLAIMS

Each of the following groups of Claims, as contained in the attached Appendix, are independently patentable, and the rejected Claims of these groups stand or fall together for the reasons more clearly set forth hereinbelow:

Group I	Claims 1-3
Group II	Claim 4
Group III	Claims 5, 6 and 7
Group IV	Claims 8-10
Group V	Claim 11
Group VI	Claims 12-14
Group VII	Claims 15-17
Group VIII	Claims 18-20

Group I contains Claims 1-3 which stand or fall together.

Group II contains Claim 4. Claim 4 recites that the timer includes an exclusive OR gate which receives the bus activity indicator signal and failsafe signal as inputs and wherein the output of the exclusive or deactivates the timeout signal. This additional feature is not shown or suggested by the references of record and provides a significant improvement over the prior art by providing a elegant and simple solution to the problem.

Group III contains Claims 5-7. Claim 5 cites a device that further comprises a delay device coupled between the window comparator and the failsafe indicator gate to delay arrival of the failsafe signal at the failsafe indicator gate for the delay time. Having a delay between the output of the window comparator and the failsafe indicator is now known or suggested by the references of record and avoids a critical timing issue.

Group IV contains Claims 8-10. Claim 8 is an independent system claim whereas Claim 1 is an apparatus claim. Claims 8-10 stand or fall together.

Group V contains Claim 11. Claim 11 recites an exclusive OR gate that receives a timer reset signal and the indicator signal as inputs and the output of the exclusive OR gate initiates activation of the timeout signal. Claim 11 is dependent indirectly from Claim 8 and is therefore different from Claim 4 and provides a simple and elegant solution to the system solution.

Group VI contains claims 12-14. Claim 12 recites a delay device coupled between the fall detection device and the failsafe indicator device to delay arrival of the indicator signal at the failsafe indicator device for a delay time period. Claim 12 is dependent from Claim 8 and therefore different from Claim 5. Having a delay circuit on the indicator signal in a system of Claim 8 is not shown or suggested by the references of record and avoids a critical timing issue.

Group VII contains claims 15-17. Claim 15 is a method of providing failsafe detection in a differential receiver circuit and is therefore, different from Claims 1 and 8. Claims 15-17 stand or fall together.

Group VIII contains claims 18-20. Claim 18 is dependent upon Claim 15 and includes the utilization of an exclusive OR gate to commence the countdown time periods including the exclusive OR gate receiving indications of both threshold transitions. This feature is not shown in a method by the references of record. Claims 18-20 stand or fall together.

ARGUMENTS

The Examiner rejects claims 1-4, 8-11 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over APA in view of Erckert, U. S. Patent 6,493,401.

We cannot agree. Referring to the bottom of column 3 through column 4 of Erckert, it is clear that the circuits COMP1a and COMP1b perform the same function as the signal transition detector shown in Figure 1 of the present application. Thus, although the circuit configuration is different, the output of the circuit is the timer reset signal which appears on line 11 in both the APA and the present invention. Accordingly, combining Erckert with the APA would result only in a different circuit for generating the timer reset signal on line 11, and not for providing two signals to the activity timer as in the present invention, the Examiner's statements to the contrary notwithstanding. Secondly, the timer utilized in Erckert is not utilized to control the output to provide a failsafe indicator signal, as in the present invention.

There are two times in the functioning of the circuit when the detector detecting when the signals drops below a failsafe threshold will produce erroneous results. The first of these is when there is a signal transition, where the threshold detector will detect the data signal transitioning through the threshold. The second condition is when there is noise present on the line, which noise is of sufficient amplitude to drive one of the input signals below the failsafe threshold for a short period of time. The result is, if the activity timer has timed out, that the failsafe detector will cause a transition in the output, which transition is an error, since no valid data has been presented. In order to avoid this unwanted consequence of the failsafe detector, the present invention resets the activity timer on both the occurrence of data and the occurrence of noise or other false indications on the line so that a fault condition is only detected both the activity timer

times out and the fault condition still exists. This overcomes the problem of the prior art by eliminating the possibility that noise on the line will cause the device to issue an erroneous data signal or erroneously place the output at a predetermined state. There is no showing or suggestion in either of the APA or Erckert of this problem, or a solution thereto.

The Examiner rejects claims 5-7, 12-14, 19 and 20 under 35 U.S.C. 103 (a) as being unpatentable over the APA and Erckert in view of Shirai et al., U.S. Patent 5,867,775.

The Examiner admits that Erckert does not show the delay circuit coupled between the window comparator and the failsafe indicator circuit. The Examiner's statement that Erckert shows a switch that changes after a timer expires fails to mention that this is for an entirely different purpose. Shirai discloses a timer circuit in a transmitter, not a receiver, and the circuit delays a fault signal that indicates a failure in a DC voltage supply, and not a fault condition on a differential data bus.

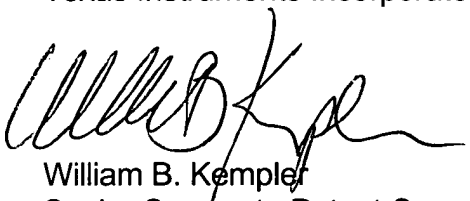
Applicant's do not claim the utilization of a time delay to a failsafe indicator in the abstract. In the present invention the delay is utilized to allow the activity timer to be reset before the output of the window comparator is applied to the failsafe indicator, which avoids a critical timing issue. In view of the fact that the references of record, either singly or in combination, fail to disclose the timing problem, they do not, either singly or in combination show or suggest the solution, the Examiner's statements to the contrary not withstanding.

CONCLUSION

For the above reasons, Applicants respectfully submit that the Examiner's Final Rejection of the Claims under 35 U.S.C. § 102, 35 U.S.C. § 102(a) and 35 U.S.C. § 103(a), are not properly founded in law. Applicants respectfully request that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections of the Claims.

Respectfully submitted,

Texas Instruments Incorporated



William B. Kempler
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APPENDIX

1. An apparatus for providing failsafe detection for a differential receiver that produces a bus activity indicator signal when receiving a differential data signal of sufficient amplitude to transition through a first predetermined receiver threshold, said apparatus comprising:

a window comparator having an input coupled to said differential receiver and operable to activate a failsafe signal when a transition below a second predetermined threshold occurs on said differential receiver, said second predetermined threshold being less than said first predetermined threshold;

a timer coupled to said window comparator and having an input to receive said bus activity indicator signal and said failsafe signal, said timer operable for deactivating a timeout signal in response to each activation of said bus activity indicator signal and said failsafe signal, said timer further for activating said timeout signal if a predetermined period of time elapses since a most recent deactivation of said timeout signal; and

a failsafe indicator gate coupled to said timer and said window comparator to receive said timeout signal and said failsafe signal, and having an output to set a flag when said failsafe signal and said timeout signal are both active.

2. The apparatus of Claim 1, wherein said failsafe indicator gate comprises an OR gate.

3. The apparatus of Claim 1, wherein said window comparator further comprises:

first and second comparators configured to compare said differential data signal with respective first and second references, wherein said first and second references are at said second threshold and represent a failsafe threshold; and

a logic gate coupled to said comparators to receive outputs from said comparators.

4. The apparatus of Claim 3, wherein said timer includes an exclusive OR gate which receives said bus activity indicator signal and failsafe signal as inputs, and wherein an output of said exclusive OR deactivates said timeout signal.

5. The apparatus of Claim 1, further comprising a delay device coupled between said window comparator and said failsafe indicator gate to delay arrival of said failsafe signal at said failsafe indicator gate for a delay time period.

6. The apparatus of Claim 5, wherein said delay time period exceeds an amount of time required for said timer to deactivate said timeout signal.

7. The apparatus of Claim 6, wherein said delay device comprises an RC circuit.

8. A system for providing failsafe detection in a differential receiver network, said system comprising:

a differential input device configured to provide a timer reset signal upon receiving a differential data signal of sufficient amplitude to transition through a predetermined receive threshold;

a fault detection device coupled to said differential input device and configured to provide an indicator signal when said differential data signal transitions into a fault threshold region, said fault threshold being less than said receive threshold;

a resetable timer coupled to said differential input device and said fault detection device and configured to provide a timeout signal upon expiration of a predetermined amount of time after receiving either said timer reset signal or said indicator signal; and

a failsafe indicator device coupled to said timer and said fault detection device and configured to set a flag when said indicator signal persists following expiration of said amount of time.

9. The system of Claim 8, wherein said failsafe indicator device comprises an OR gate which receives said timeout signal and said indicator signal as inputs.

10. The system of Claim 8, wherein said fault detection device further comprises:

first and second comparators configured to compare said differential data signal with respective first and second references, wherein said first and second references are at said fault threshold and represent a failsafe threshold; and

a logic gate coupled to said comparators to receive outputs from said comparator.

11. The system of Claim 10, wherein said timer includes an exclusive OR gate that receives said timer reset signal and said indicator signal as inputs, and wherein an output of said exclusive OR gate initiates activation of said timeout signal.

12. The system of Claim 8, further comprising a delay device coupled between said fault detection device and said failsafe indicator device to delay arrival of said indicator signal at said failsafe indicator device for a delay time period.

13. The system of Claim 12, wherein said timer is operable for initially deactivating said timeout signal upon receiving either said timer reset signal or said indicator signal, and wherein said delay time period exceeds an amount of time required for said timer to deactivate said timeout signal.

14. The system of Claim 13, wherein said delay device comprises an RC circuit.

15. A method of providing failsafe detection in a differential receiver circuit, said method comprising;

comparing a differential data signal received by said differential receiver circuit to a predetermined receive threshold , said failsafe threshold being less than said receive threshold, and commencing a countdown time period upon detecting a receive threshold transition;

comparing said differential data signal to a predetermined failsafe threshold and commencing a countdown time period upon detecting a failsafe threshold transition; and

setting an indicator flag upon detecting a failsafe threshold transition following expiration of one of the countdown time periods.

16. The method of Claim 15, wherein said setting step includes using an OR gate to set said indicator flag, and including said OR gate receiving indications of both of said threshold transitions.

17. The method of Claim 15, wherein said setting step includes using a first logic gate to set said indicator flag, and including said first logic gate receiving indications of both of said threshold transitions, and wherein said commencing steps include using a second logic gate to commence the countdown time periods, and including said second logic gate receiving indications of both of said threshold transitions.

18. The method of Claim 15, wherein said commencing steps include using an exclusive OR gate to commence the countdown time periods, and including said exclusive OR gate receiving indications of both of said threshold transitions.

19. The method of Claim 15, including providing a failsafe condition indication in response to said first-mentioned detecting step, said second-mentioned detecting step including delaying said failsafe condition indication for a delay period of time.

20. The method of Claim 19, wherein said delay period exceeds an amount of time required for commencement of one of the countdown time periods after detection of the corresponding threshold transition.